1. A process for removing a layer of silicon oxynitride, comprising:

providing a substrate and depositing thereon a layer of silicon oxynitride;

mounting said substrate on a platen and, using a polishing pad and a slurry, removing said layer of silicon oxynitride, thereby forming a fresh surface;

removing said polishing pad and then washing off any remaining slurry; and

with said substrate still on the platen, subjecting said fresh surface to a high pressure rinse by a solution that comprises a surfactant that modifies hydrophobic behavior, thereby removing from said fresh surface any and all residual particles of silicon oxynitride.

2. The process described in claim 1 wherein said solution that comprises a surfactant has a pH between about 8 and 11.

3. The process described in claim 1 wherein said surfactant is present in said solution at a concentration of between about 2 and 10 weight percent.

4. The process described in claim 1 wherein said fresh surface is subjected to said high pressure rinse for between about 5 and 20 seconds.

5. A process for removing a layer of silicon oxynitride, comprising:

providing a substrate and depositing thereon a layer of silicon oxynitride;

mounting said substrate on a platen and, using a polishing pad and a slurry, removing said layer of silicon oxynitride, thereby forming a fresh surface;

removing said polishing pad and then washing off any remaining slurry; and

with said substrate still on the platen, subjecting said fresh surface to a high pressure rinse by a solution that comprises tetramethyl ammonium hydroxide, thereby removing from said fresh surface any and all residual particles of silicon oxynitride.

6. The process described in claim 5 wherein said solution that comprises tetramethyl ammonium hydroxide has a pH between about 8 and 11.

7. The process described in claim 5 wherein tetramethyl ammonium hydroxide is present in said solution at a concentration of between about 2.5 and 5 weight percent.

8. The process described in claim 5 wherein said fresh surface is subjected to said high pressure rinse for between about 5 and 20 seconds.

9. A process for removing a layer of silicon oxynitride, comprising:

providing a substrate and depositing thereon a layer of silicon oxynitride;

mounting said substrate on a platen and, using a polishing pad and a slurry, removing said layer of silicon oxynitride, thereby forming a fresh surface;

removing said polishing pad and then washing off any remaining slurry; and

with said substrate still on the platen, subjecting said fresh surface to a high pressure rinse by a solution that comprises isopropyl alcohol, thereby removing from said fresh surface any and all residual particles of silicon oxynitride.

10. The process described in claim 9 wherein said solution that comprises isopropyl alcohol has a pH between about 8 and 11.

11. The process described in claim 9 wherein isopropyl alcohol is present in said solution at a concentration of between about 10 and 50 weight percent.

12. The process described in claim 9 wherein said fresh surface is subjected to said high pressure rinse for between about 5 and 20 seconds.

13. A process for forming a tungsten stud in a silicon integrated circuit, comprising:

providing a partially completed integrated circuit whose top layer is conductive;

on said conductive layer, depositing a dielectric layer;

on said dielectric layer, depositing a layer of silicon oxynitride;

on said layer of silicon oxynitride, depositing a layer of titanium nitride;

patterning and then etching said titanium nitride, silicon oxynitride, and dielectric layers to form a via hole that extends as far as said conductive layer;

over-filling said via hole with tungsten whereby a layer of tungsten, having a first

thickness, covers said titanium nitride layer;

on a first platen, subjecting said tungsten layer to CMP until a second thickness of tungsten covers said titanium nitride layer;

on a second platen, subjecting said integrated circuit to CMP until all tungsten outside said via hole has been removed and until said layer of titanium nitride has also been removed;

on a third platen, subjecting said integrated circuit to CMP, using a polishing pad and a slurry, until said layer of silicon oxynitride has been removed, thereby forming a fresh surface;

removing said polishing pad and then washing off any remaining slurry; and

with said integrated circuit still on said third platen, subjecting said fresh surface to a high pressure rinse by a solution that comprises a surfactant that modifies hydrophobic behavior, thereby removing from said fresh surface any and all residual particles of silicon oxynitride.

14. The process described in claim 13 wherein said solution that comprises a surfactant has a pH between about 8 and 11.

15. The process described in claim 13 wherein said surfactant is present in said solution at a concentration of between about 2 and 10 weight percent.

16. The process described in claim 13 wherein said fresh surface is subjected to said high pressure rinse for between about 5 and 20 seconds.

17. The process described in claim 13 wherein the step of subjecting said fresh surface to a high pressure rinse further comprises emitting said solution that comprises a surfactant from a dispenser at a flow rate between about 100 and 300 ml/min.

18. The process described in claim 13 wherein said layer of silicon oxynitride has a thickness between about 300 and 1,500 Angstroms.

19. A process for forming a tungsten stud in a silicon integrated circuit, comprising:

providing a partially completed integrated circuit whose top layer is conductive;

on said conductive layer, depositing a dielectric layer;

on said dielectric layer, depositing a layer of silicon oxynitride;

on said layer of silicon oxynitride, depositing a layer of titanium nitride;

patterning and then etching said titanium nitride, silicon oxynitride, and dielectric layers to form a via hole that extends as far as said conductive layer;

over-filling said via hole with tungsten whereby a layer of tungsten, having a first thickness, covers said titanium nitride layer;

on a first platen, subjecting said tungsten layer to CMP until a second thickness of tungsten covers said titanium nitride layer;

on a second platen, subjecting said integrated circuit to CMP until all tungsten outside said via hole has been removed and until said layer of titanium nitride has also been removed;

on a third platen, subjecting said integrated circuit to CMP, using a polishing pad and a slurry, until said layer of silicon oxynitride has been removed, thereby forming a fresh surface;

removing said polishing pad and then washing off any remaining slurry; and

with said integrated circuit still on said third platen, subjecting said fresh surface to a high pressure rinse by a solution that comprises tetramethyl ammonium hydroxide, thereby removing from said fresh surface any and all residual particles of silicon oxynitride.

20. The process described in claim 19 wherein said solution that comprises tetramethyl ammonium hydroxide has a pH between about 8 and 11.

21. The process described in claim 19 wherein tetramethyl ammonium hydroxide is present in said solution at a concentration of between about 2.5 and 5 weight percent.

22. The process described in claim 19 wherein said fresh surface is subjected to said high pressure rinse for between about 5 and 20 seconds.

23. The process described in claim 19 wherein the step of subjecting said fresh surface

to a high pressure rinse further comprises emitting said solution that comprises tetramethyl ammonium hydroxide from a dispenser at a flow rate between about 100 and 300 ml/min.

24. The process described in claim 19 wherein said layer of silicon oxynitride has a thickness between about 300 and 1,500 Angstroms.

25. The process described in claim 19 wherein said dielectric layer is silicon oxide.

26. A process for forming a tungsten stud in a silicon integrated circuit, comprising:

providing a partially completed integrated circuit whose top layer is conductive;

on said conductive layer, depositing a dielectric layer;

on said dielectric layer, depositing a layer of silicon oxynitride;

on said layer of silicon oxynitride, depositing a layer of titanium nitride;

patterning and then etching said titanium nitride, silicon oxynitride, and dielectric layers to form a via hole that extends as far as said conductive layer;

over-filling said via hole with tungsten whereby a layer of tungsten, having a first thickness, covers said titanium nitride layer;

on a first platen, subjecting said tungsten layer to CMP until a second thickness of tungsten covers said titanium nitride layer;

on a second platen, subjecting said integrated circuit to CMP until all tungsten outside said via hole has been removed and until said layer of titanium nitride has also

been removed;

on a third platen, subjecting said integrated circuit to CMP, using a polishing pad and a slurry, until said layer of silicon oxynitride has been removed, thereby forming a fresh surface;

removing said polishing pad and then washing off any remaining slurry; and

with said integrated circuit still on said third platen, subjecting said fresh surface to a high pressure rinse by a solution that comprises isopropyl alcohol, thereby removing from said fresh surface any and all residual particles of silicon oxynitride.

27. The process described in claim 26 wherein said solution that comprises isopropyl alcohol has a pH between about 8 and 11.

28. The process described in claim 26 wherein isopropyl alcohol is present in said solution at a concentration of between about 10 and 50 weight percent.

29. The process described in claim 26 wherein said fresh surface is subjected to said high pressure rinse for between about 5 and 20 seconds.

30. The process described in claim 26 wherein the step of subjecting said fresh surface to a high pressure rinse further comprises emitting said solution that comprises isopropyl alcohol from a dispenser at a flow rate between about 100 and 300 ml/min.

31. The process described in claim 26 wherein said layer of silicon oxynitride has a thickness between about 300 and 1,500 Angstroms.

32. The process described in claim 26 wherein said dielectric layer is silicon oxide.